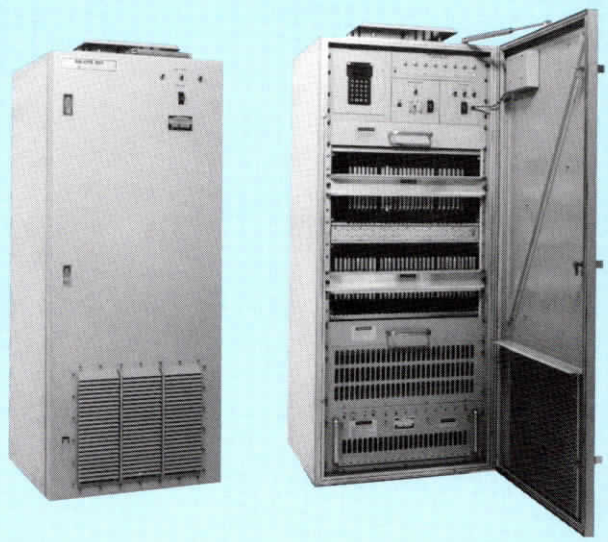
AN/UYS-501 DIGITAL PROCESSOR

ASW DIVISION

WORLD'S FASTEST MILITARIZED SHIPBORNE SIGNAL PROCESSOR



The AN/UYS-501 is a militarized High Speed Digital Processor which is designed to meet current and future computation-intensive requirements.

GENERAL CONCEPT

The AN/UYS-501 Digital Signal Processor belongs to a family of computers known as array processors and has been designed to process arrays of data in an optimal manner.

The AN/UYS-501 is a Single Instruction Multiple Data (SIMD) stream machine and the high computation speeds are achieved through a massively parallel structural design which allows many operations to be performed simultaneously. Its performance is also enhanced by its pipeline architecture which executes arithmetic operations and routes data movements concurrently. In addition, high-speed cache memories are used to buffer data between the large, slower working memory and the fast arithmetic modules. By utilizing eight identical arithmetic modules in parallel, it is able to reduce the execution time of a vector operation by a factor of eight.

The full MIL-SPEC AN/UYS-501 is contained in a single 24-inch EIA standard rack-mounted cabinet. 59 SHINPADS-size (266 mm x 250 mm) circuit card assemblies (CCAs) are accommodated in two card-files inside the cabinet. The major components of the AN/UYS-501 are the Communications Controller (Master Controller), Input/Output Interfaces, Transfer and Arithmetic Controllers, Working Memory, Cache Memory and the Arithmetic Modules.

The full MIL-SPEC AN/UYS-501 signal processor is in production and forms part of the AN/SQS-510 and AN/SQR-501 sonar systems.

The AN/UYS-501 is extremely efficient and can be easily programmed to implement kernel digital signal processing operations such as FFTs, heterodyning, frequency-domain beamforming, vector dot products and other vector operations. A large variety of data array reorderings such as cornering, bit-reversal and order-reversal can be accomplished with no performance penalty.

INTERNAL OPERATION

The communications controller is the control executive processor of the AN/UYS-501. It utilizes the Motorola MC68020 microprocessor and governs the activities of the Input/Output (I/O) interfaces and the transfer and arithmetic controllers.

Up to five independent signal processor I/O interfaces (16-bit parallel, STANAG 4153 or High-Speed Serial Interface), one tape recorder interface, and five RS-232C serial interfaces are provided by the AN/UYS-501. The signal processor I/O interfaces are used to access the working memory for data transfers. One of the five RS-232C interfaces is dedicated for use as the host interface and the other four are used as general-purpose communication links between the communications controller and external devices. A host computer is connected to the AN/UYS-501 via the host interface and is used to download application programs and to initiate and terminate the communications controller software.

The transfer controller's role is to control the data flow between the working memory and the cache memory. The arithmetic controller controls the operations taking place between the arithmetic modules and the cache memory. Conceptually, each controller can be divided into two halves: the left- and the right-halves. The left-halves of the two controllers are identical; they communicate with the communications control and set up the address and mode registers for their right-halves. The right-halves act as slaves to their corresponding left-halves. The right-half of the transfer controller controls the data movement between the working memory and cache memory. The right-half of the arithmetic controller controls the arithmetic operations that are taking place in the arithmetic modules. The left-half/right-half split allows the next transfer or arithmetic operation to be set up in the left-half while the right-half executes current instructions. This reduces housekeeping and overhead and allows for more efficient computing.

The working memory contains 4M 64-bit words (IEEE 754 floating-point complex) of dynamic RAMs and is divided into eight segments. Addresses separated by 2^n ($0 \leq n \leq 15$) locations are stored in different segments so that they can be accessed in parallel.

The cache memory contains 32K 64-bit words of fast static RAMs and is divided into two sets, each containing 16K 64-bit words. One set is connected to the working memory and the other set is connected to the arithmetic modules. The role of the sets is interchanged by the transfer and arithmetic controllers. The sets of the cache memory are also segmented to permit parallel access to multiple words.

There are eight arithmetic modules in the AN/UYS-501. Each module consists of an arithmetic unit which performs complex or 32-bit real word operations in the form of $A \pm BC$, a functions unit which may or may not map the arithmetic unit data by a mode or function, an expanded heterodyne facility unit which provides coefficient memory addresses to the corresponding arithmetic unit for beamforming and heterodyning. Data is processed in an arithmetic pipeline, with data moving synchronously and concurrently in the cache memory and arithmetic modules.

Both on-line and off-line diagnostics provide an excellent degree of fault isolation to the card level.

GENERAL SPECIFICATION

DIMENSIONS

Height	1651 mm (65 in.)
Width	680.7 mm (26.8 in.)
Depth	688 mm (27 in.)

WEIGHT

260 Kg (573 lbs)

ENVIRONMENTAL CONDITIONS

Temperature	Operating	0°C to 50°C
	Nonoperating	-62°C to 71°C

POWER REQUIREMENTS

Input Voltage	115 V AC
Frequency	60 Hz
Phase	Single
Power Consumption	1.5 KVA maximum

COOLING

Forced Air

MTBF

The MTBF of the AN/UYS-501, (according to MIL-HDBK-217E) will not be less than 600 hours for the naval-sheltered environment at an ambient temperature of 25 °C.

MTTR

30 minutes maximum

DIAGNOSTIC CAPABILITIES

Off-Line	> 80% of faults to a single card > 90% of faults to two cards > 95% of faults to four cards
On-Line	> 90% of all hard faults will be detected

TAPE RECORDER INTERFACE

Quantity	One
Type	Interface to either of the full MIL-SPEC recorders
	Ampex DCRSI Ground System
or	Honeywell TMR fixed two-speed machine

SIGNAL PROCESSOR INTERFACES

Quantity	Maximum of five
Type and Data Rates	Each interface can be software configured to be a:
	16-bit parallel with a maximum average data rate of 1.85M 16-bit words/s. Maximum burst rate is 2M 16-bit words/s
or	STANAG 4153 serial interface, using 32-bit word transfers, at a maximum rate of 153,000 32-bit words/s
or	High-speed serial interface at a maximum rate of 10M bits/s.

SERIAL INTERFACES

Quantity	Five RS-232C serial interfaces
Type and Data Rates	Each serial interface data rate is programmable with the maximum rate being 19.2K baud.

WORKING MEMORY CAPACITY

32 M bytes of DRAM expandable to 512 M bytes.

CACHE MEMORY CAPACITY

256 K bytes of Static RAM expandable to 512 K bytes.

PERFORMANCE

Speed	320 Mflops (million floating-point operations per second) sustained. 1K complex FFT in 160 µs.

FUNCTIONS

Hardware Implemented (no performance overhead)	Modes are DIV2, ZIP and REAL. Functions are signum, absolute value, reciprocal, square root, log (base 2), or antilog (base 2)
Software Implemented (approx. 500 ns per argument when spread over 8 arithmetic units).	Functions are sine, cosine, arcsine, arccosine and arctangent

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